second storage circuit is coupled to the first storage circuit and configured to deactivate the first storage circuit based on the second bit.

Montoye discloses a CAM cell having match logic 102 coupled to a pair of storage cells 301, 302 (Fig. 3) that each stores a single bit. However, as confirmed by a simple inspection of the schematic of Fig. 3, neither of these cells is deactivated based on the bit stored at the other one of these bit cells. There is simply no signal path that causes one of cells 301, 302 to be deactivated based on the bit stored in the other of cells 301, 302. In other words (and just as in art cited in the previous office action), the bit stored in one of the bit cells 301, 302 of Montoye has no effect on whether the other one of the bit cells is deactivated. Thus, Montoye fails to teach or suggest a second storage circuit configured to deactivate the first storage circuit based on the second bit, as recited in claim 1.

The Office Action refers to specific portions of Montoye, none of which teach or suggest this claim recitation. The Office Action refers to col. 3, lines 29-67 and col. 4, lines 1-34. This portion does mention that various transistors in match logic 102 may be turned off, however this is irrelevant to whether cell 301 or cell 302 is deactivated. More precisely, this portion of Montoye does not teach or suggest deactivating one of the cells 301, 302 based on the bit stored in the other cell. In stark contrast, referring to the example of Fig. 2 in Applicant's own specification, storage circuit 214 is deactivated based on the bit stored at node 231 of storage circuit 213 (via transistor 212).

For at least these reasons, it is submitted that claim 1 is allowable over Montoye.

Independent Claim 6

Independent claim 6 recites an apparatus, comprising a plurality of dual-bit memory cells. Each claimed memory cell includes (1) a first storage circuit configured to store a first bit, (2) a second storage circuit configured to store a second bit, (3) a first plurality of word lines each controlling one of the first storage circuits, and (4) a second plurality of word lines each controlling one of the second storage circuits. In addition, the first storage circuit includes a transistor having a gate, and the gate is coupled to the second storage circuit so as to receive a

value of the second bit.

The Office Action attempts to compare elements of claim 6 with Montoye as follows:

Element of Claim 6	Examiner's Comparison in Montoye (Fig. 4)
first storage circuit	301
second storage circuit	302
first plurality of word lines	/ML
second plurality of word lines	ML
transistor	304

Applicants respectfully submit that the above comparison in the Office Action is in error. First, in Montoye, match lines /ML and ML are not word lines; they are match lines. Instead, word line W is the word line. See Fig. 4; col. 3, lines 39-40 and col. 4, lines 53-54. Where the claimed first and second word lines are properly compared with of Figs. 3 and 4 of Montoye, it can be seen that Montoye only has a single word line W for the pair of storage cells 301, 302. Thus, Montoye fails to teach or suggest *both* the first and the second plurality of word lines in the configuration claimed.

Montoye additionally fails to teach or suggest the claimed transistor. Claim 6 recites that the gate of the transistor is coupled to the second storage circuit so as to receive a value of the second bit. This is not the case in Montoye. Instead, the gate of transistor 304 is connected to word line W, which clearly does not provide the value of the second bit (i.e., using the Examiner's comparison, the bit stored in storage cell 302). Thus, the gate of transistor 304 does not receive the value of the second bit, as claimed. In stark contrast, referring to the example of Fig. 2 in Applicant's own specification, storage circuit 214 has a transistor 212, which has a gate coupled to storage circuit 213 so as to receive a value of the bit stored at node 231.

For at least these reasons, it is submitted that claim 6 is allowable over Montoye.

Dependent Claims

The remaining dependent claims are also allowable as they depend from allowable claim 6, and further in view of the additional features recited therein.

Conclusion

All rejections having been addressed, it is submitted that the claims are in condition for immediate allowance, and notice to that effect is respectfully solicited. Should the Examiner feels that a telephone call or personal interview would be beneficial to the examination of this application, the Examiner is invited to contact the undersigned at the number below.

Respectfully submitted,

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